METHOD AND STRUCTURE FOR PMOS DEVICES WITH HIGH K METAL GATE INTEGRATION AND SIGE CHANNEL ENGINEERING

RELATED APPLICATIONS

This application is a divisional of U.S. Ser. No. 12/367,759, filed Feb. 9, 2009, the entire contents of which are incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates to a semiconductor structure and a method of fabricating the same. More particularly, the present invention relates to a semiconductor structure for a p-type metal oxide semiconductor (MOS) including a high k gate dielectric and an engineered SiGe channel and methods of fabricating the same.

BACKGROUND OF THE INVENTION

In the quest for improved semiconductor device performance, semiconductor circuits are becoming denser and the semiconductor devices located therein are becoming smaller. For example, the most common dielectric in MOS field effect transistors has been SiO_2. However as the thickness of SiO_2 approaches 15 angstroms, substantial problems appear, including, for example, leakage currents through the gate dielectric, concerns about the long-term dielectric reliability, and the difficulty in manufacturing and thickness control.

One solution to the above problem is to use thick (greater than 20 angstroms) films of materials, such as hafnium oxide (HfO_2), that have a dielectric constant that is larger than SiO_2, e.g., high k gate dielectrics. Thus, the physical thickness of the high k gate dielectric can be large, while the electrical equivalent thickness relative to SiO_2 films can be scaled.

Introduction of high k gate dielectrics, such as HfO_2, ZrO_2 or Al_2O_3, in gate stacks has proven to reduce leakage current by several orders of magnitude. Such leakage current reduction has enabled the fabrication of complementary metal oxide semiconductor (CMOS) devices with lower power consumption.

It is also desirable to replace Si-containing gates with metal gates that give a workfunction near the band edge for both nMOS and pMOS devices. A number of metal gates are known for nMOS devices, however, metal gates for pMOS devices are rarer.

As such, there is an ongoing need for providing pMOS devices that include a high k gate dielectric in which the workfunction thereof is near the band edge for pMOS devices which does not necessarily have to rely solely on a p-type workfunction metal.

SUMMARY OF THE INVENTION

The invention provides a solution to the above problem by changing the workfunction of the substrate to SiGe rather than Si which changes the bandgap favorably for subsequent fabrication of pMOS devices. Although such a solution has been proposed in the past, the actual building of such devices has been rare and extremely difficult. Moreover, in order to get a strong threshold voltage shift (Vt) for current metals a reasonable high Ge content (greater than 30 atomic %) was previously used. High Ge content SiGe films suffer from defect formation as well as eroision, pitting and rough surfaces, all of which degrade the pMOS mobility.

The present invention provides various means for changing the workfunction of the substrate by using a SiGe channel which, in turn, changes the bandgap favorably for a p-type metal oxide semiconductor field effect transistor (pMOSFET). The invention includes providing a SiGe film that includes a low doped SiGe region above a more highly doped SiGe region to allow the appropriate threshold voltage (Vt) for pMOSFET devices while preventing pitting, roughness and thinning of the SiGe film during subsequent cleans and processing.

In general terms, a method of fabricating a substrate including an engineered SiGe channel that is suitable for pMOSFET devices is provided which includes:

providing a semiconductor substrate having at least one active area with an exposed upper surface; and

forming a SiGe film on the exposed upper surface of the active area, said SiGe film including a lower region that has a first Ge concentration and an upper region that has a second Ge concentration, wherein the first Ge concentration is greater than the second Ge concentration.

In one embodiment, the forming of the SiGe film includes the formation of an oxide cap on the surface of an initial SiGe layer. During the formation of the oxide cap, the Ge content within the SiGe layer diffuses downward away from the interface of the growing oxide cap. After the oxide cap is stripped, a silicon (Si) cap is formed on the remaining SiGe layer. In this embodiment, the combination of the Si cap and the oxidized and stripped SiGe layer represents the SiGe film mentioned above. That is, the Si cap represents an upper region of the SiGe film that has less Ge than the lower region which is represented by the oxidized and stripped SiGe layer.

In another embodiment, the forming of the SiGe film includes forming a Si cap on an initial SiGe layer and thereafter subjecting the structure to a heating process that causes the formation of the SiGe film.

In yet another embodiment, the SiGe film is formed by forming a SiGe cap having a low Ge content on a surface of an initial SiGe layer that has a high Ge content.

In an even further embodiment, the SiGe film is formed by providing an in-situ doped cap in an upper surface of an initial SiGe layer.

In a still further embodiment, the SiGe film is formed by providing a graded SiGe film whose Ge content decreases upwardly from an interface with the underlying substrate.

The present invention also provides a structure including an engineered SiGe channel that includes:

a semiconductor substrate having at least one active area with an exposed upper surface; and

a SiGe film located on the exposed upper surface of the active area, the SiGe film including a lower region that has a first Ge concentration and an upper region that has a second Ge concentration, wherein the first Ge concentration is greater than the second Ge concentration.

In some embodiments of the invention, the aforementioned structure further includes a high k gate dielectric and a gate conductor located atop the SiGe film. In a highly preferred embodiment, the high k gate dielectric and the gate conductor are elements of a pMOS.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A-**1**E are pictorial representations (through cross sectional views) depicting the basic processing steps in accordance with a first embodiment of the invention.

FIGS. **2**A-**2**B are pictorial representations (through cross sectional views) depicting the basic processing steps in accordance with a second embodiment of the invention.